Cgo

PATENT

I he shy certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 18, 2007

Denise Sheridan

Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paul R. Petersen Attorney Docket No.: 188906/US/2 (M00-175100)

Patent No. : 7,251,618 B2 Serial No. : 09/733,372

Issue Date: July 31, 2007 Filed: December 8, 2000

Title : METHOD AND SYSTEM FOR PURCHASING A MEMORY UPGRADE FOR A

COMPUTER SYSTEM

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Certificate

DEC 2 8 2007

of Correction

Sir:

A Certificate of Correction under 35 U.S.C. § 254 is respectfully requested for the above-identified patent. Some of the errors were made in the printing of the patent while others were made in the original application. The changes in the patent needed to correct the errors are as follows:

Column, Line	Reads	Should Read
Column 3, Line 48	"the 12C bus"	the I2C bus
Column 3, Lines 64-65	"memory controller 110"	memory controller 108
Column 4, Line 42	"200 may stored in"	200 may be stored in
Column 4, Line 43	"memory controller 110"	memory controller 108

Column 4, Lines 48- "memory controller 110" --memory controller 108--49

The errors are considered sufficiently important to justify the processing of a Certificate of Correction under 35 U.S.C. § 254. A Form PTO-1050, in duplicate, is enclosed herewith.

The Commissioner is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 50-1266. A duplicate copy of this sheet is enclosed.

Favorable consideration of this Request is respectfully requested.

Respectfully submitted,

Date: Dec. 14, 2007

Bv:

Edward W. Bulchis, Reg. No. 26,847

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Attorney for Applicant(s)

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Enclosures:

Postcard

Form PTO-1050 (+ copy)

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

7,251,618 B2

DATED

July 31, 2007

INVENTOR(S)

Paul R. Petersen

It is certified that error appears in the above identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Column 3, Line 48	"the 12C bus"	the I2C bus
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		-
Column 4, Lines 48-49	"memory controller 110"	memory controller 108

MAILING ADDRESS OF SENDER:

Patent No. 7,251,618 B2

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